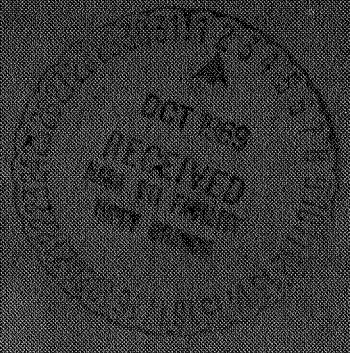
FINAL REPORT

TO: National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama



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FAIRCHILD
SEMICONDUCTOR

SQ-259 060R

TEST AND INSPECTION FOR PROCESS CONTROL OF MONOLITHIC CIRCUITS

Final Technical Report

Fairchild Semiconductor

November 1966

Contract No. NAS8-21011

Prepared For:

National Aeronautics and Space Administration
George C Marshall Space Flight Center
Huntsville, Alabama

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ILLUSTRATIONS

SECTION I

INTRODUCTION

This document was prepared under the technical cognizance of the Fairchild Semiconductor Director of Reliability. The technical project leader was Mr. Jay Farley, the Reliability Manager for Integrated Circuits. The manual draws heavily upon present and historical achievements of Fairchild technical personnel and their ability to mass-produce highly reliable semiconductor devices.

The manual is keyed to a process flow chart for Diode-Transistor Logic (DTL) integrated circuits, particularly the Fairchild Semiconductor Low-Power Diode-Transistor Micrologic (LPDTμL) family, which consists of a set of compatible, integrated logic circuits specifically designed for low power, medium-speed applications. (This circuit family features reliable operation over the full military temperature range of -55°C to 125°C and is thus well suited to line qualification for NASA applications.) Each process step is listed, giving the number of the manufacturing specification controlling the step. These specifications form the nucleus of the document and are keyed directly to the flow chart.

Emphasis is placed on process control and every item of equipment is described in terms that assure rigid quality control. All critical inspection and process stations are highlighted, both in the process flow chart and in the accompanying text. Measurements, tests, inspections, and calibration procedures are detailed.

This document reflects the manufacturing state-of-the-art at Fairchild and describes only those process steps which are presently being used up till 15 November 1966. The manual is written in a manner to clearly present the information and to ensure full understanding by typical production-line personnel of the procedures required and the expected results.

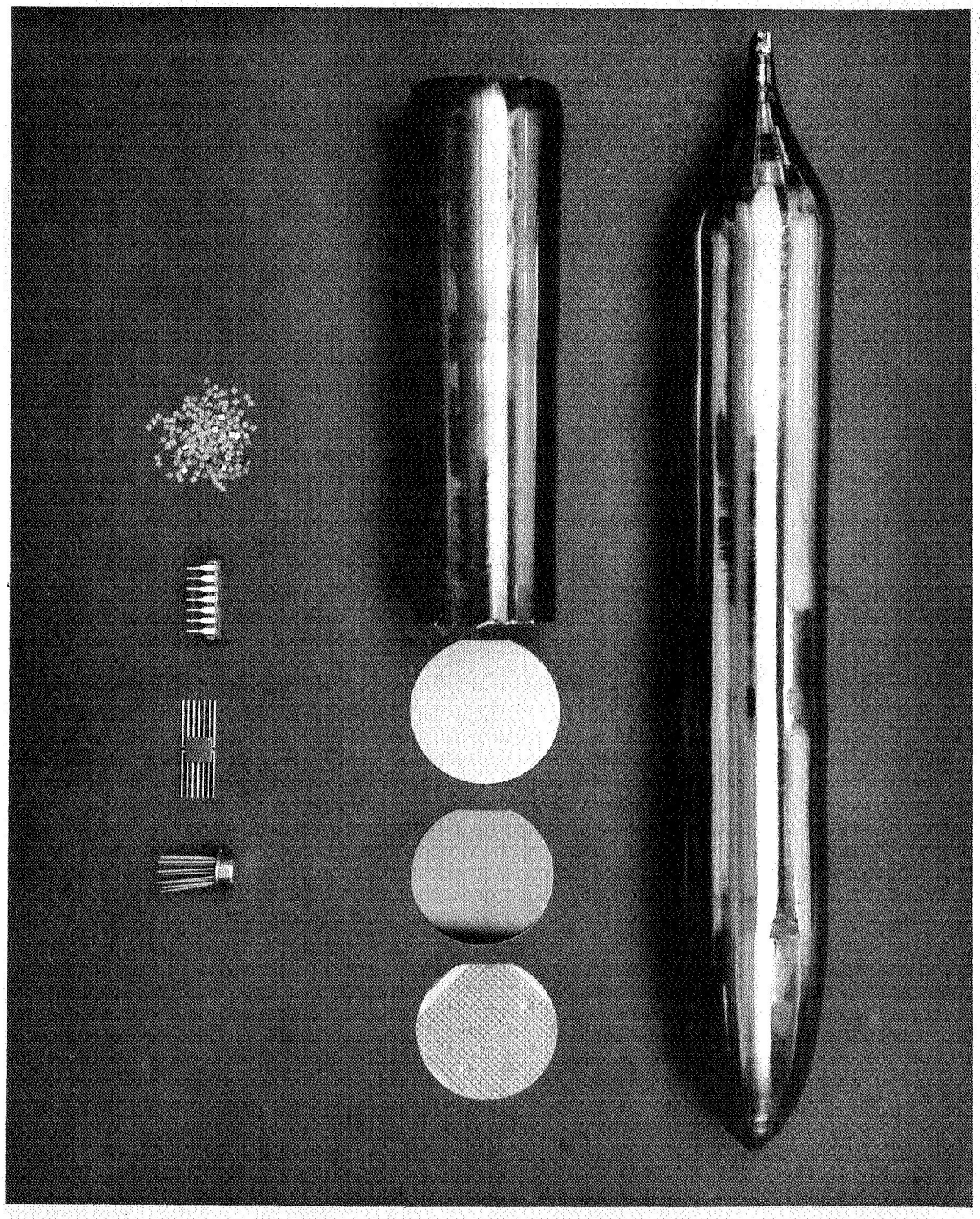


Fig. 1 Steps in the Manufacture of Integrated Circuits

SECTION II

CIRCUIT DESCRIPTION

The Fairchild LPDTμL Micrologic® Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications. The circuits are fabricated with a silicon monolithic substrate using standard Fairchild Planar epitaxial processes. The circuits are packaged in either flat package or dual in-line package.

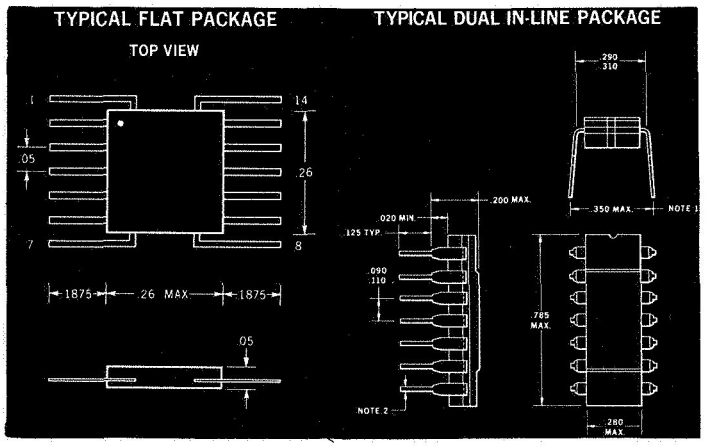


Fig. 2 Typical DTL Packages

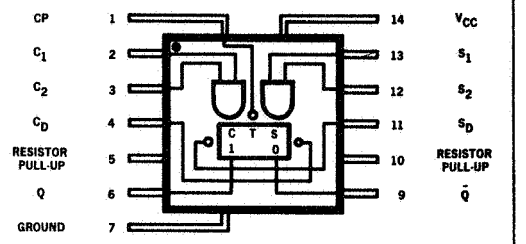
This section contains data on the Fairchild LPDTμL Micrologic® Integrated Circuit Family; specifically the 9040, 9041, and 9042.

LPDTμL 9040 CLOCKED FLIP-FLOP

DESCRIPTION

The LPDTμL 9040 element is a directly coupled, dual-rank flip-flop suitable for use in counters, shift registers and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN LINE PACKAGE PIN ASSIGNMENT



SYNCHRONOUS ENTRY TRUTH TABLES

R-S MODE OPERATION

INPUTS @t_n				OUTPUTS @t_{n+1}	
S_1	S_2	C_1	C_2	Q	$\bar{Q}$
13	12	2	3	6	9
L	X	L	X	NC	NC
L	X	X	L	NC	NC
X	L	L	X	NC	NC
X	L	X	L	NC	NC
L	X	H	H	L	H
X	L	H	H	L	H
H	H	L	X	H	L
H	H	X	L	H	L
H	H	H	H	AMBIGUOUS	

J-K MODE OPERATION

INPUTS @t_n		OUTPUTS @t_{n+1}	
S_1	C_1	Q	$\bar{Q}$
13	2	6	9
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	TOGGLES	

ASYCHRONOUS ENTRY TRUTH TABLE

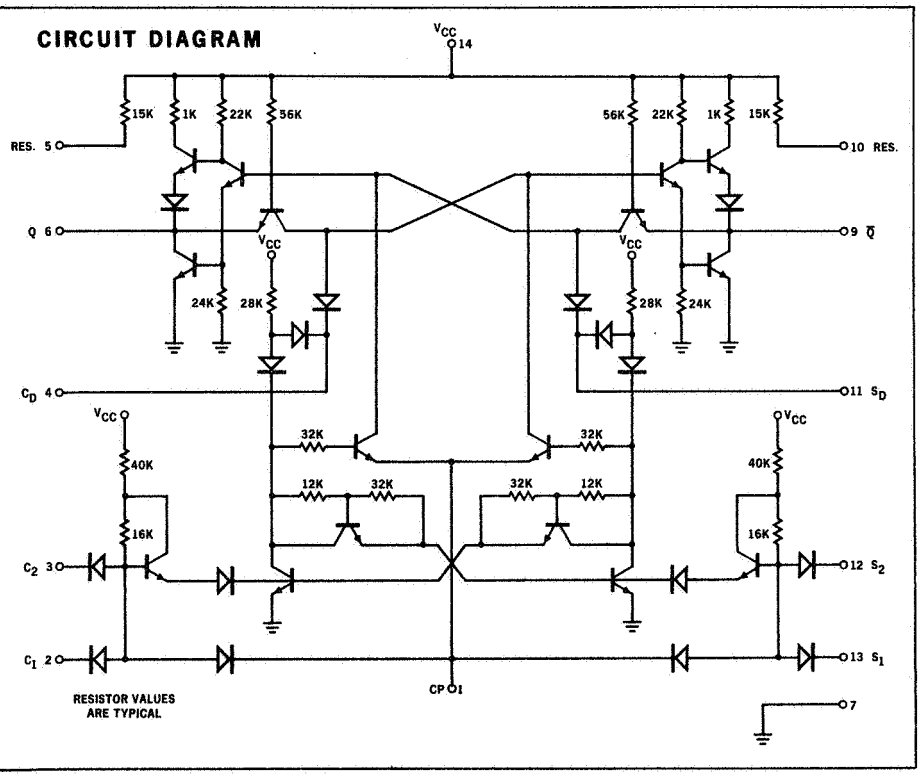
INPUTS		OUTPUTS	
S_D	C_D	Q	$\bar{Q}$
11	4	6	9
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

Symbols

H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC - No change in state

NOTES:
1. For J-K mode operation connect Pin 6 to Pin 3 and Pin 9 to Pin 12.
2. Asynchronous entries override all synchronous entries.

CIRCUIT DIAGRAM



LOADING RULES

INPUT	*NORMALIZED UNIT LOADS (U.L.)
S_1 S_2 C_1 C_2	0.75 U.L.
S_D C_D	2.5 U.L.
CP	2.5 U.L.
OUTPUT	**FAN-OUT**
Q, $\bar{Q}$	10 U.L. 7 U.L. WITH RESISTOR PULL-UP CONNECTED

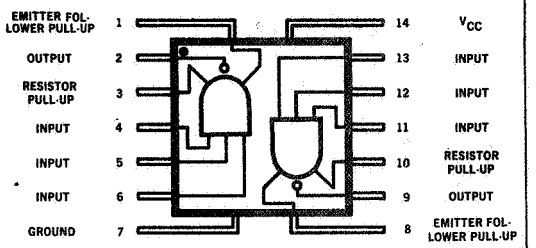
*1UNIT LOAD EQUALS 1-LPDTμL 9041 OR 9042 INPUT LOAD

LPDTμL 9041 — DUAL 3 INPUT NAND GATE

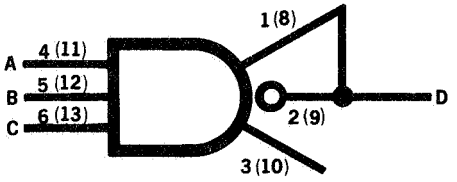
DESCRIPTION

The LPDTμL 9041 element consists of two, 3-input positive logic NAND gates suitable for general logic gate and inverter applications. The unique feature of this gate is that the output transistor collector and the emitter follower pull-up are not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT



POSITIVE LOGIC NAND GATE



$\overline{ABC} = D$

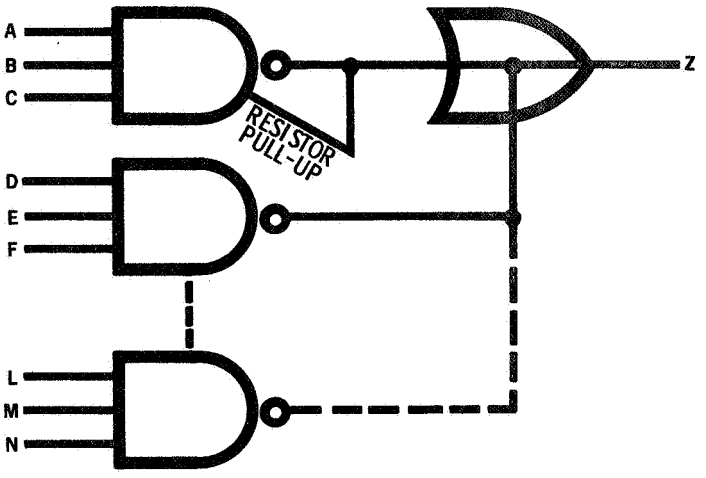
EACH INPUT = 1 UNIT LOAD

OUTPUT FAN-OUT = 10 UNIT LOADS

= 7 U.L. WITH RESISTOR PULL-UP CONNECTED

EITHER THE EMITTER FOLLOWER OR RESISTOR PULL-UP MUST BE CONNECTED TO THE OUTPUT TO ESTABLISH THE HIGH LEVEL.

WIRED 'OR' APPLICATION

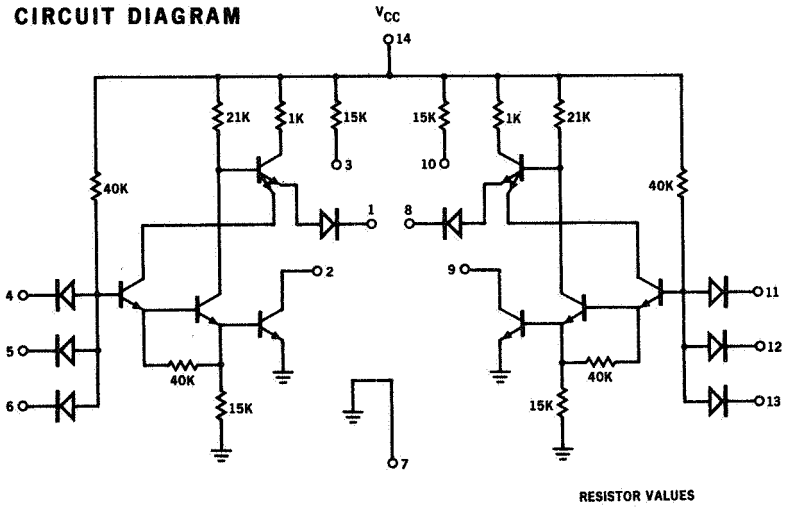


$\overline{ABC + DEF + \cdots + LMN} = Z$

OUTPUT FAN-OUT = 10 - 3 (NO. OF RESISTOR PULL-UPS)

ONE PULL-UP RESISTOR IS REQUIRED FOR EVERY 13 GATES CONNECTED TO THE COMMON "OR" NODE.

CIRCUIT DIAGRAM



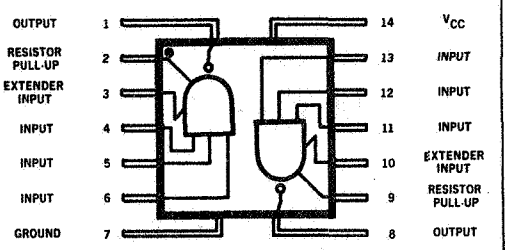
LPDTμL 9042 — DUAL 3 INPUT NAND GATE WITH EXTENDER INPUTS

DESCRIPTION

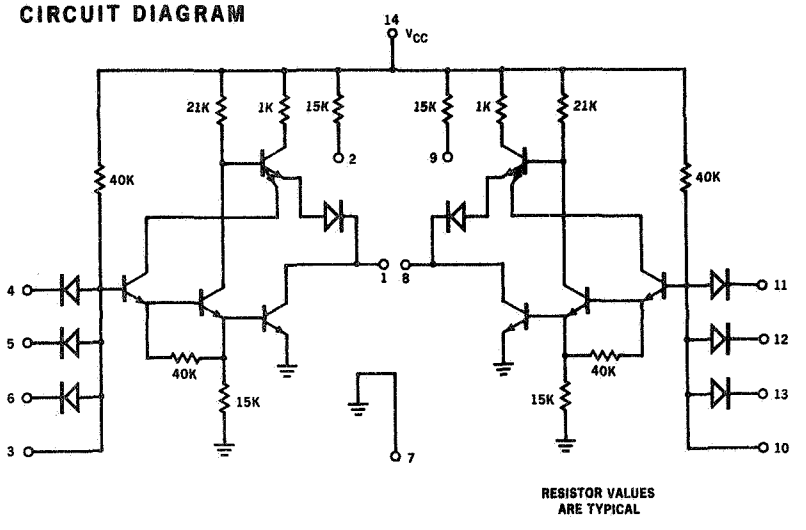
The LPDTμL 9042 element consists of two 3-input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan-in exceeding three.

The DTμL 9933 4-input extender element or equivalent—may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTμL 9042 gate. Typically, the increase is 10 ns/pico-farad. Turn-off delay is not affected.

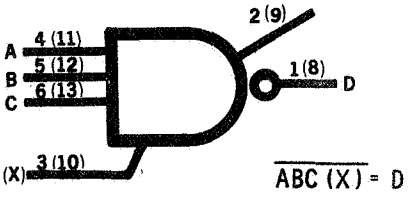
LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT



CIRCUIT DIAGRAM



POSITIVE LOGIC NAND GATE



$\overline{ABC}$ (X) = D

EACH INPUT = 1 UNIT LOAD

OUTPUT FAN-OUT = 10 UNIT LOADS

= 7 UNIT LOADS WITH RESISTOR PULL-UP CONNECTED

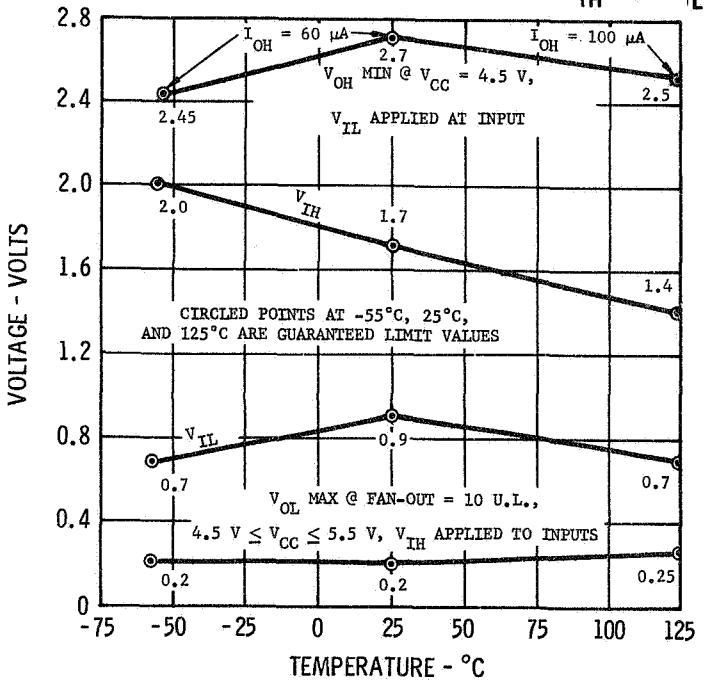
BUFFER ELEMENT

For applications requiring a fan-out exceeding ten, the Fairchild DTμL 9930 Dual 4-Input Gate may be used. The DTμL 9930 will drive 44 LPDTμL unit loads, while maintaining the same output logic levels as the low power circuits.

The input of a DTμL 9930 requires the equivalent of 10 LPDTμL unit loads. Therefore, a low power circuit can drive only one DTμL 9930 input.

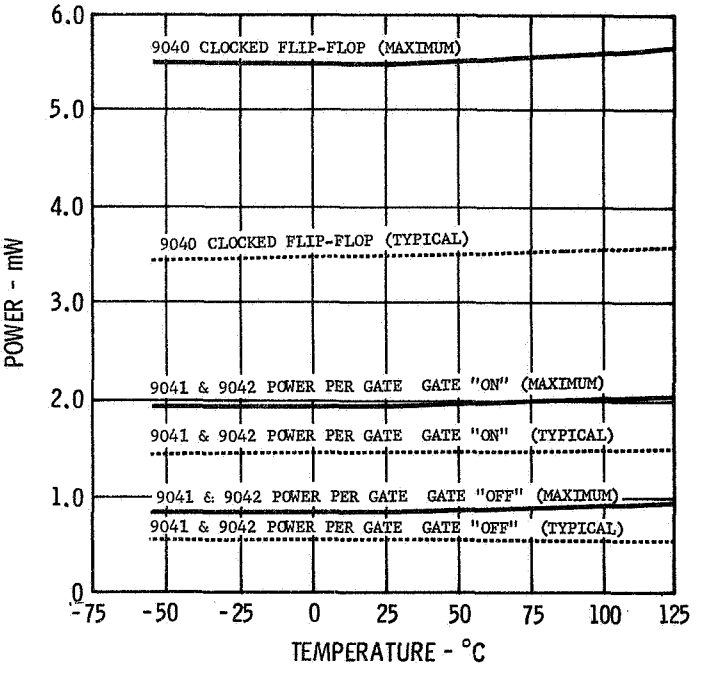
OPERATING VOLTAGE CHARACTERISTICS

WORST CASE OUTPUT LOGIC LEVELS - V_{OH} AND V_{OL}
INPUT THRESHOLD LEVELS - V_{IH} AND V_{IL}

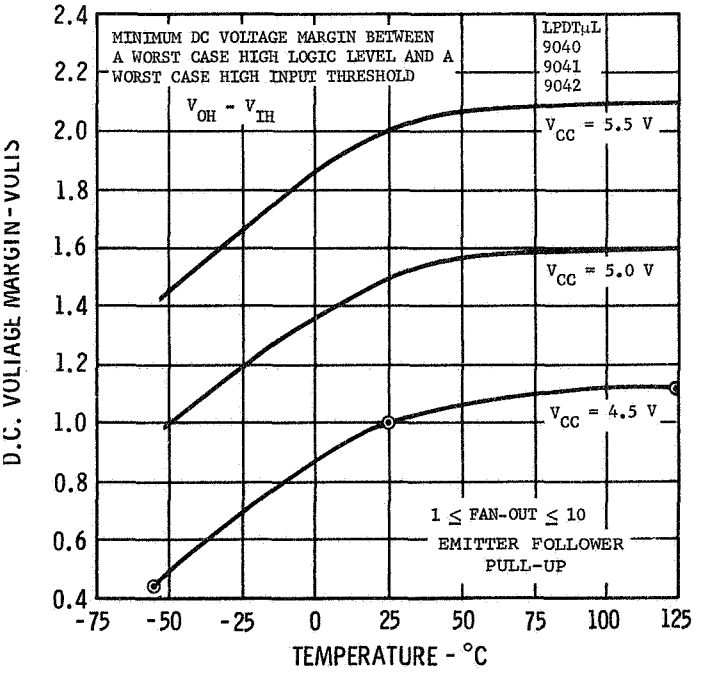


POWER CHARACTERISTICS

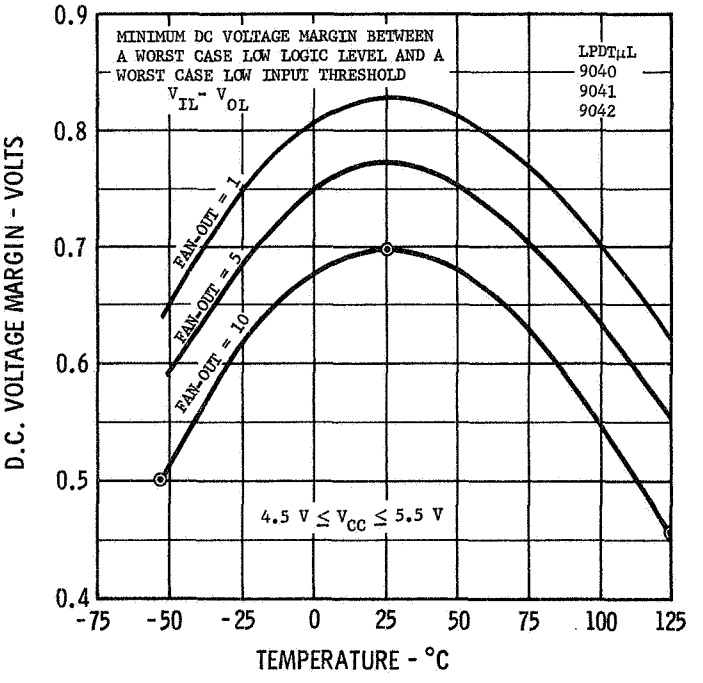
VCC = 5V
EMITTER FOLLOWER PULL-UP



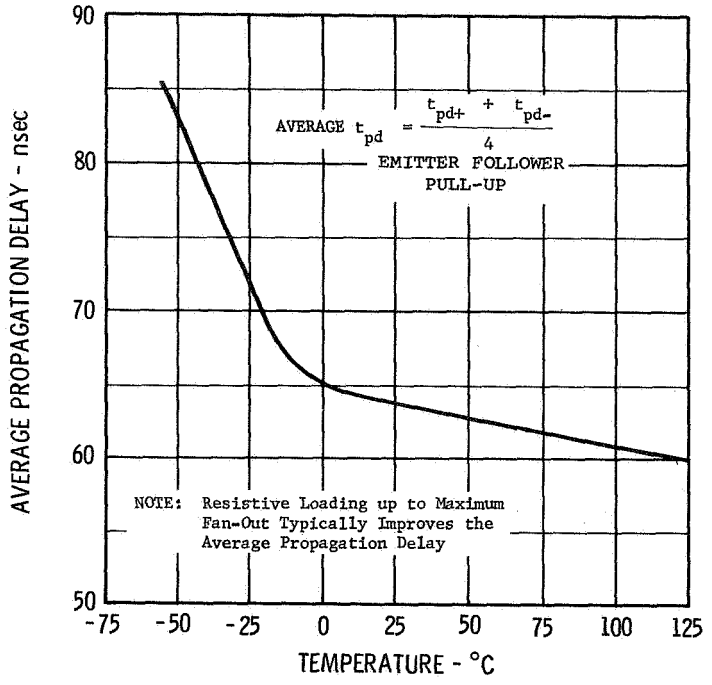
HIGH LEVEL NOISE IMMUNITY



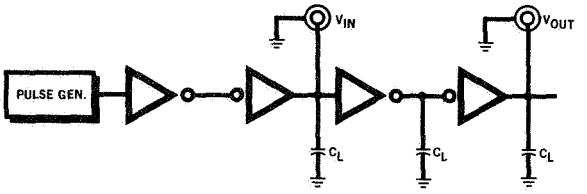
LOW LEVEL NOISE IMMUNITY



TYPICAL AVERAGE PROPAGATION DELAY LPDTμL 9041 • 9042



TEST CIRCUIT

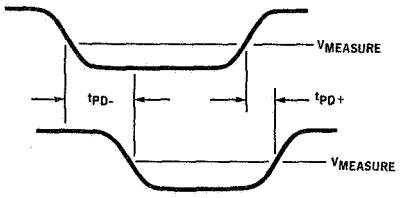


CONDITIONS

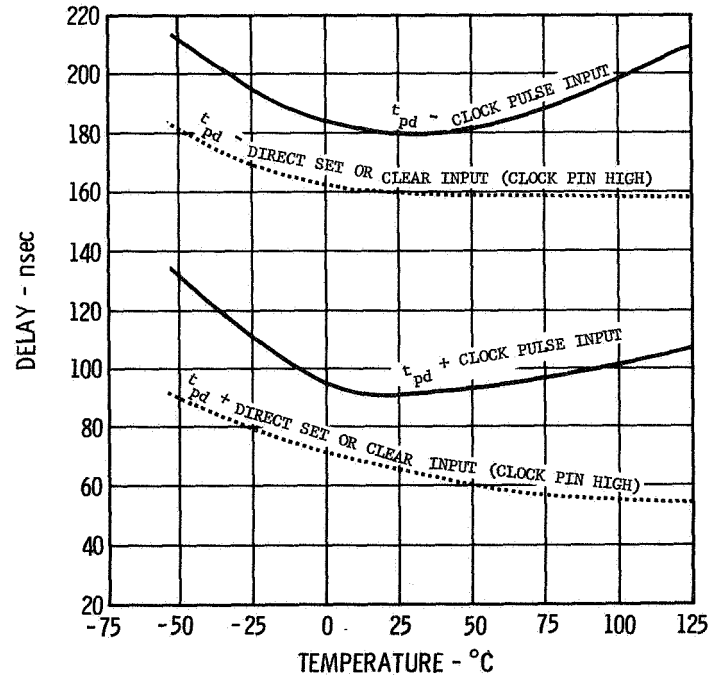
V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITANCE)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

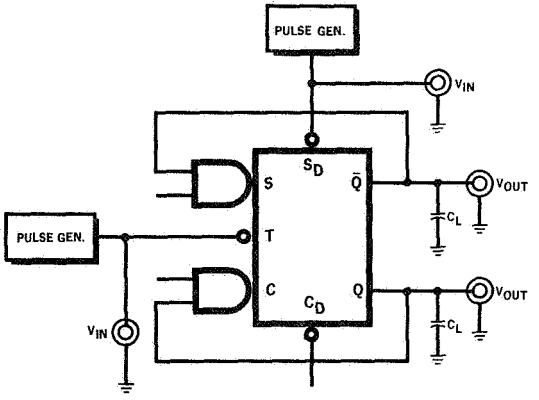
WAVE FORMS



TYPICAL DELAY CHARACTERISTICS LPDTμL 9040



TEST CIRCUIT



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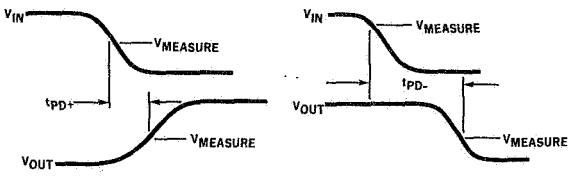
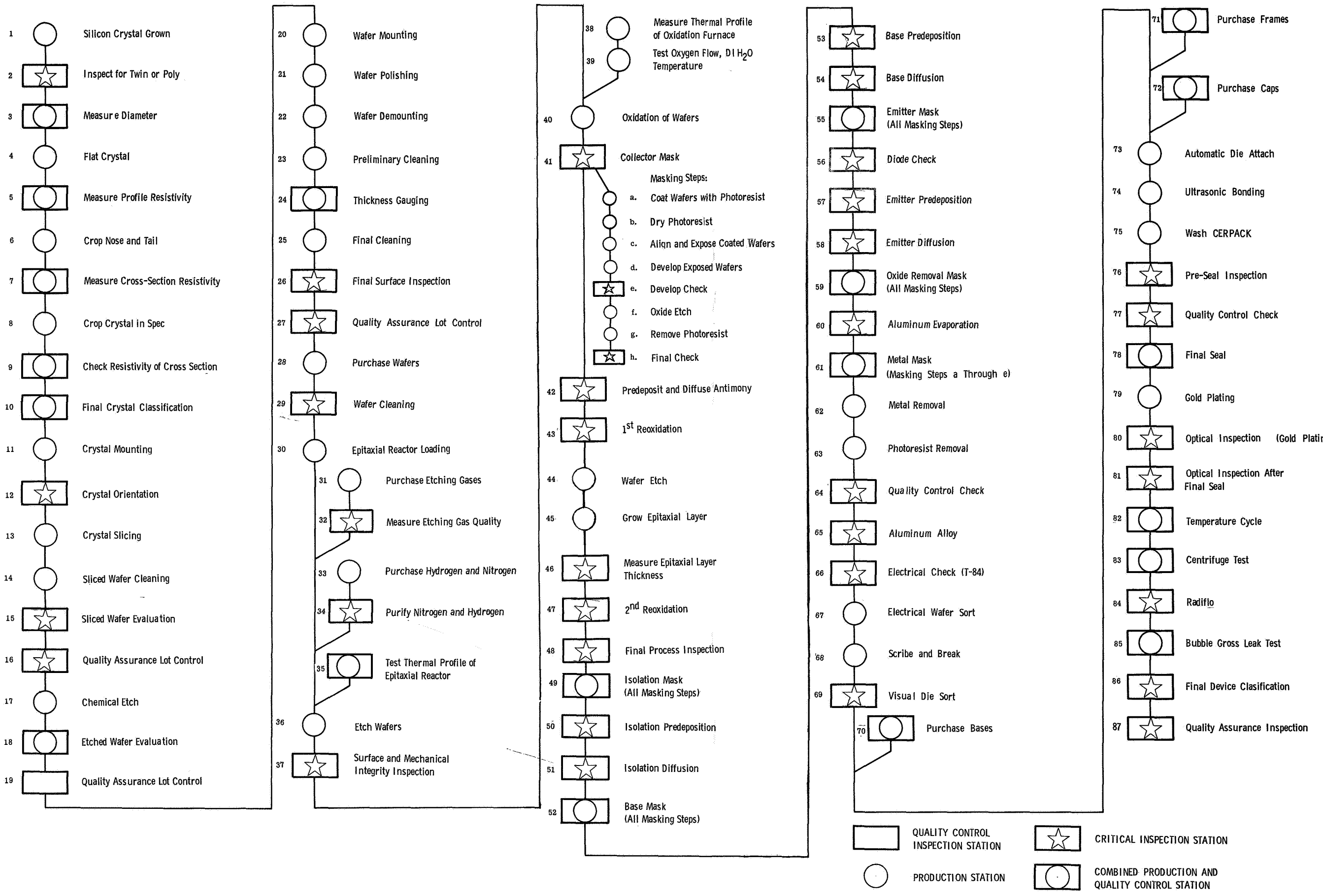
WAVE FORMS





PROCESS FLOW CHART FOR DTL CIRCUITS

SECTION III

PROCESS FLOW CHART

The process flow chart is keyed to the following text which describes each step in the manufacture of DTL integrated circuits. The title of each process or inspection step is followed by the number of the Fairchild manufacturing specification controlling that step. Critical inspection stations are called out and all equipment is listed.

PROCESS STEPS

1. Silicon Crystal Grown (2300) Rev. O dated 11-30-64

   A poly-silicon charge and dope are placed in a quartz crucible. The crucible is placed in the carbon susceptor of a Fairchild Furnace (Fairchild Dwg. No. 21960) which is then sealed, purged with argon and heated to 1450° C. When the charge and dope have reached a molten state, a silicon seed is introduced into the melt and a crystal is grown from this seed as it is slowly pulled from the melt.

2. Inspect for Twin or Poly (2300) Rev. O dated 11-30-64

   THIS IS A CRITICAL INSPECTION STATION. The grown crystal, when removed from the furnace, is inspected for twin or poly lines. POLY WAFERS CANNOT BE USED FOR MONOLITHIC CIRCUITS. If twin or poly lines are found while the crystal is still in the furnace, the crystal can be remelted to the origin of the lines. A twin or poly crystal, once out of the furnace, is rejected.

3. Measure Diameter

   All crystals are gauged to assure that they are within the proper diameter range. Under-diameter crystals are rejected and

over-diameter crystals are ground in a centerless grinder to bring them to the proper specifications. The grinder used is a type C-4 manufactured by Engleberg-Huller. The gauge plate is manufactured by Fairchild and is routinely checked against standard scales.

4. Flat Crystal (2306) Rev. O dated 1-11-66

A 3/8 in. to 5/8 in. flat surface is ground along the full length of the crystal. The flat surface is ground relative to given orientation lines on a Fairchild Flatting Machine (Dwg. No. 71000-100). The diamond wheel of the Flatting Machine is periodically checked for wear.

5. Measure Profile Resistivity (2302) Rev. O dated 12-8-65

The flat of the crystal is probed with a Four-Point Probe (Si-0626, A and M Fell, Ltd.), connected to a Constant Current Generator (Fairchild No. 1506-03), Amplifier (Hewlett-Packard 425AR), and a Digital Voltmeter (Fairchild No. 7100); all incorporated into a Fairchild manufactured resistivity test jig. The operator probes the crystal every inch of its length and records the resistivity readings. This measurement is made only to determine where to crop the crystal. If no part of the crystal falls within the resistivity specifications the crystal is rejected. All electronic devices are periodically calibrated by Fairchild's Electronic Services Group and equipment is checked daily with a set of standards.

6. Crop Nose and Tail (2303) Rev. O dated 11-2-65

The crystal is placed in a Cut-Off Machine (Nav-Kut, Navan Products, Inc.) and the nose and tail are cropped where the crystal is within the proper diameter range. Crystal diameter and profile resistivity readings determine the cropping points. Constant visual surveillance is maintained on the condition of the diamond wheel of the Cut-Off Machine.

7. Measure Cross-Section Resistivity (2302) Rev. O dated 12-8-65

Cross-sections of the crystal are measured with the same equipment as used in step no. 5. The operator probes the nose and tail of the crystal and records the resistivity readings. This measurement is taken to determine whether further cropping is necessary.

8. Crop Crystal in Spec. (2303) Rev. O dated 11-2-65

The pre-marked crystal is placed in the Navan Cut-Off Machine and the operator saws the crystal along the marks.

9. Check Resistivity of Cross-Section (2302) Rev. O dated 12-8-65

Sections of the cropped crystal are probed on the cross-section to ensure that they are within the proper resistivity range. Equipment used for this check is the same as that used in step no. 5. If none of the crystal section falls within the specified resistivity range the section is rejected.

10. Final Crystal Classification

Each length of crystal is labeled with the device number for which the crystal was grown, length, weight, resistivity readings, crystal number, and inspector's name. This information is recorded on a data sheet and the crystals are shipped to the next process department.

11. Crystal Mounting (2404) Rev. O dated 8-13-65

The single silicon crystal is etched for 20 minutes in 5N NaOH and honed with 100 grit abrasive in an Abrasive Blast Unit (Industrial Cleaning Machines, Model 3600). The crystal is then bonded to an aluminum Crystal Holding Billet (Fairchild manufactured) using wax with a high melting point. Slice support slabs of silicon are attached to each crystal by the mounting wax. If there is any visual evidence of poor bonding, the crystal is removed from the holding billet, cleaned of wax, and re-bonded.

12. Crystal Orientation (2409) Rev. O dated 7-20-66

THIS IS A CRITICAL INSPECTION STATION. Each mounted crystal is mechanically secured to an Alignment Jig (Do-All Equipment Inc.) and optically oriented in collimated light in such a manner as the 1, 1, 1 crystal plane is misoriented by 2° - 3° parallel to the Diamond Saw Blade (Do-All Equipment Inc.). After cutting the first slice, the orientation is checked using an X-Ray Diffraction Instrument (Siemens and Haiske, Model No. 176121A). Readjustment of the alignment is made as required to provide slices orientated 2° 30' ± 30 off the 1, 1, 1 crystal plane. SLICE ORIENTATION AFFECTS EPITAXIAL DEPOSITION CHARACTERISTICS AND SUBSEQUENT MASKING PROPERTIES FOR CIRCUIT FABRICATION. The Light Fixture used is manufactured by Fairchild.

13. Crystal Slicing (2401) Rev. O dated 9-27-65

The single crystal silicon, mounted and oriented as previously described, is sliced into wafers 240μ - 450μ in thickness. Over-thickness material may be lapped or etched to correct thickness. Under-thickness material is scrapped. The Slicing Machine is a Do-All MicroSlicer manufactured by Do-All Equipment Inc. or a Precision Wafering Machine (Hamlo Machine and Electrical Co.).

14. Sliced Wafer Cleaning (2405) Rev. O dated 2-24-66

Sliced wafers are ultrasonically cleaned in an aqueous alkaline detergent bath and air dried. A 1000 watt Ultrasonic Tank and Generator (Crest Ultrasonics) is used. Thic cleaning process if for manufacturing ease only.

15. Sliced Wafer Evaluation (2403) Rev. O dated 9-24-65

THIS IS A CRITICAL INSPECTION STATION. Each sliced wafer is electronically type tested for p or n material, visually inspected for surface defects, gauged for thickness and sorted into 5μ thickness groups. resistivity tested, counted, packed and identified for manufacturing lot and type of material. SLICED WAFERS MUST MEET RESISTIVITY SPECIFICATIONS AT THIS STAGE OF MANUFACTURE IN ORDER TO PRODUCE THE DESIRED MONOLITHIC CIRCUIT ELECTRICAL CHARACTERISTICS.

Wafers which are not in resistivity specifications are scrapped. The equipment used is 4-point resistivity instrumentation (Fairchild manufactured), type test instrumentation (Fairchild manufactured), and a mechanical thickness gauge (Federal Gauge, Inc.). Standard thickness strips are supplied by Quality Assurance. All instrumentation is checked daily by Fairchild's Electronic Services Group.

16. Quality Assurance Lot Control (Sliced Wafers)
(4008) Rev. O dated 11-9-66

THIS IS A CRITICAL INSPECTION STATION. Sliced wafers are inspected to assure that the material is not defective. The sliced wafers are sampled to a 4% AOQL. THE SLICED WAFER MUST BE CORRECTLY IDENTIFIED AS TO RESISTIVITY AND TYPE (N or P). ALSO, SLICE ORIENTATION MUST BE CORRECT FOR EPITAXIAL DEPOSITION. The equipment used is a Thickness Gauge (Federal Gauge Co.), a Resistivity Meter manufactured by Fairchild, and a Type Tester manufactured by Fairchild.

17. Chemical Etch (2604) Rev. O dated 9-14-66

Each sliced wafer is chemically etched in an acid mixture to remove surface damage resulting from the slicing operation. After etching, each wafer is rinsed and dried. This preparation step is done for manufacturing east os subsequent operations. The Chemical Etch Reactor is manufactured by Fairchild.

18. Etched Wafer Evaluation (2604) Rev. O dated 9-14-66

Each etched wafer is inspected visually for stains, fractures, epi chips, and other surface damage. Each wafer is then gauged for thickness, packed, counted, and the lot is identified for material type, lot number and count. Wafers which are over or under the $\pm 10\mu$ specification tolerance, fractured, or display visually any surface damage deeper than 20μ are scrapped; wafers over target thickness are re-etched. The Thickness Gauge used is manufactured by Federal Gauge, Inc.

19. Quality Assurance Lot Control (Etched Wafers) (4008) Rev. O dated 11-9-66

Etched wafers are inspected to assure that there are no defects. Wafers are sampled to a 4% AOQL.

20. Wafer Mounting (2601) Rev. O dated 11-24-65

Each wafer is mounted on a Metal Carrier (Fairchild manufactured). Bonding between the Carrier and the wafer is accomplished using a high melting point wax. Wafer height is adjusted by varying the amount of adhesive wax between the Carrier and the wafer. Equipment used is a 1600 watt Hol Plate (Thermoylene Inc. No. 2200) and a Depth Gauge with a dial indicator reading 0 to 1000μ in one μ increments (Starret Tool Inc.).

21. Wafer Polishing (2601) Rev. O dated 11-24-65

Mounted wafers are polished on Lapidary Polishing Machines (Highland Park, Inc.) using one μ diamond paste, cleaned ultrasonically to remove the one μ polish abrasive and polished to finished specification on Lapidary Polishing Machines using a 1/2 μ or less proprietary polishing media. Underpolished material is re-polished; over polished material is scrapped. A 200 watt Ultrasonic Cleaning Tank and Generator (Acoustics Associated Inc.) is used.

22. Wafer Demounting (2601) Rev. O dated 11-24-65

The Mounted wafers and carrier are heated until the mounting wax softens. The polished wafers are then removed and placed in cleaning boats. Broken wafers are discarded. A 1600 watt Hot Plate (Acoustics Associated Inc. No. 2200) is used.

23. Preliminary Cleaning (2601) Rev. O dated 11-24-65

Demounted wafers are cleaned of mounting wax by either alkaline aqueous solutions in a 1000 watt Ultrasonic Cleaning System (Acoustica Associated Inc.), or by vapor degreasing with dichloro methane in a Two-Compartment Degreaser (Branson Instrument Inc.). This cleaning is made to facilitate wafer thickness gauging.

24. Thickness Gauging (2601) Rev. O dated 11-24-65

Each wafer is gauged for final thickness using an Electronic Probe Gauge (Federal Gauge Inc. No. 100B-48.). The gauge is checked daily to standard thickness strips supplied by Quality Assurance.

25. Final Cleaning (2601) Rev. O dated 11-24-65

Each wafer is precision cleaned using an alkaline aqueous detergent solution and ultrasonic cleaning equipment. Wafers are then dried and submitted to final surface inspection processes. An Ultrasonic Cleaning Tank and a 500 Watt Generator (Acoustica Associated Inc.) are used.

26. Final Surface Inspection (2601) Rev. O dated 11-24-65

THIS IS A CRITICAL INSPECTION STATION. Each wafer is visually inspected under collimated light for surface defects and cleanliness. Acceptable wafers are counted, packed, and labeled by manufacturing lot and material type. THIS FINAL INSPECTION ASSURES POLISHED SURFACE CLEANLINESS AND FREEDOM FROM SURFACE DEFECTS SUCH AS FRACTURES, PITS, UNEVEN POLISHING AND SCRATCHES WHICH AFFECT THE FINAL ELECTRICAL CHARACTERISTICS AND THE MATERIAL IN SUBSEQUENT MANUFACTURING OPERATIONS. Material with surface defects is scrapped; contaminated material is recleaned. The Collimated Light Source is manufactured by American Optical Co.

27. Quality Assurance Lot Control (4008) Rev. O dated 11-9-66

THIS IS A CRITICAL INSPECTION STATION. The mechanically polished wafers must have a mirror finish on one side. On this surface, an epitaxial layer or oxide layer will be deposited in the next operation. THE EPITAXIAL AND/OR OXIDE LAYERS WILL CONFORM TO THE POLISHED WAFER SURFACE. It is imperative that all saw marks and scratches be removed from the polished surface. The equipment used is the same as in step no. 16.

28. Purchase Wafers (2601) Rev. O dated 11-24-65

Wafers are obtained from the Materials Department Stores. Dirty or fractured wafers are rejected after a visual inspection.

29. Wafer Cleaning (2900) Rev. O dated 9-8-65

THIS IS A CRITICAL INSPECTION STATION. Wafers are loaded into cleaning racks, dipped into hot H_2So^4 , and rinsed in de-ionized water. A HIGH DEGREE OF SURFACE CLEANLINESS IS REQUIRED FOR SUBSEQUENT EPITAXIAL PROCESSING.

30. Epitaxial Reactor Loading (2802) Rev. H dated 10-13-65

Wafers are placed upon a Silicon Carbide Coated Susceptor. They are then placed inside the Reactor tube centered in the RF coil of the epitaxial Reactor. The Silicon Carbide Coated Susceptor is manufactured by Texas Instruments, Inc.

31. Purchase Etching Gasses

Hydrogen bromide and hydrogen chloride are purchased from approved vendor sources.

32. Measure Etching Gas Quality (2602) Rev. O dated 11-22-65

THIS IS A CRITICAL INSPECTION STATION. Etching gas quality is determined by empirical tests using a 25 - 5- KW RF Generator (Westinghouse) and an Etching Reactor (Fairchild Type "C"). IMPURITIES IN ETCHING GAS MAY CAUSE PREFERENTIAL ETCHING OR SILICON AND FILM DEPOSITS.

33. Purchase Hydrogen and Nitrogen

Hydrogen and Nitrogen are purchased from approved vendor sources.

34. Purify Nitrogen and Hydrogen

THIS IS A CRITICAL INSPECTION STATION. Purchased gases are run through a Palladium Purifier (Milton Roy Co.). GASEOUS IMPURITIES WILL ALTER THE ELECTRICAL CHARACTERISTICS OF THE EPITAXIAL LAYER. IMPURITIES CAN ALSO CAUSE PREFERENTIAL ETCHING. Excessive concentrations of water vapor in the gasses are withdrawn in the Purifier.

35. Test Thermal Profile of Epitaxial Reactor (2802) Rev. A dated 10-13-65

The thermal profile of epitaxial Reactor is tested and corrected by varying the RF induction coil space and monitoring the results with an Optical Pyrometer (Precision Instruments Co.). The Optical Pyrometer is periodically calibrated by Fairchild's Electronic Services Group.

36. Etch Wafers (1926) Rev. O dated 3-18-65

After loading the wafers into the reactor, conditions of temperature and flow are set to gas etch the wafer surface. Periodic checks are made with test wafers to determine etch rates of the gasses. An Epitaxial Reactor (Fairchild Type "C") and a 25 - 50 KW RF Generator (Westinghouse) are used.

37. Surface and Mechanical Integrity Inspection (2803) Rev. O dated 10-22-65

THIS IS A CRITICAL INSPECTION STATION. All wafers are visually inspected for surface film, pitting, cracks, and fractures. THIS INSPECTION INDICATES LEAKS OR IMPROPER TEMPERATURE OF THE REACTOR.

38. Measure Thermal Profile of Oxidation Furnace (2700) Rev. O dated 8-13-65

The oxidation furnace is periodically checked to assure that the

temperature is as specified. The thermal profile of the furnace is checked with a Potentiometer and a Thermocouple manufactured by Northrup. Furnace heat inputs may be adjusted to obtain the proper thermal profile.

39. Test Oxygen Flow, Deionized H_2O Temperature

(2700) Rev. O dated 8-13-65

These parameters are periodically checked to ensure product uniformity. Oxygen is checked with a Gas Rotameter (Fischer and Porter); temperature is checked with a thermometer. Oxygen flow can be adjusted, if necessary, with a needle valve. Water temperature can be adjusted by varying the heat input of the bubbler.

40. Oxidation of Wafers (1353) Rev. F dated 12-10-63

Wafers are loaded into a Pacesetter II Oxidation Furnace (Thermco Inc.), oxidized for two hours at 1200°C and unloaded.

41. Collector Mask

MASKING STEPS

a. Coat Wafers with Photoresist (1354) Rev. C dated 11-4-64

Wafers are mounted on a Center Line Spinner and coated with photoresist, Kodak Metal Etch Resist (KMER), and rotated at a high speed.

Newton's rings indicate incomplete or nonuniform coverage of the wafers with photoresist and are cause for wafer rejection. Properly coated wafers are developed, dried and recoated. Photoresist thickness is monitored by exposing a coated bare silicon wafer with a cross line mask in a nitrogen atmosphere. The wafer is developed and interference rings are counted. Equipment used is a Volk Automatic Spinner Model II (Fairchild Manufactured), a Laminar Flow Hood (Fairchild manufactured), and Kodak Metal Etch Resist (Eastman Kodak Co.).

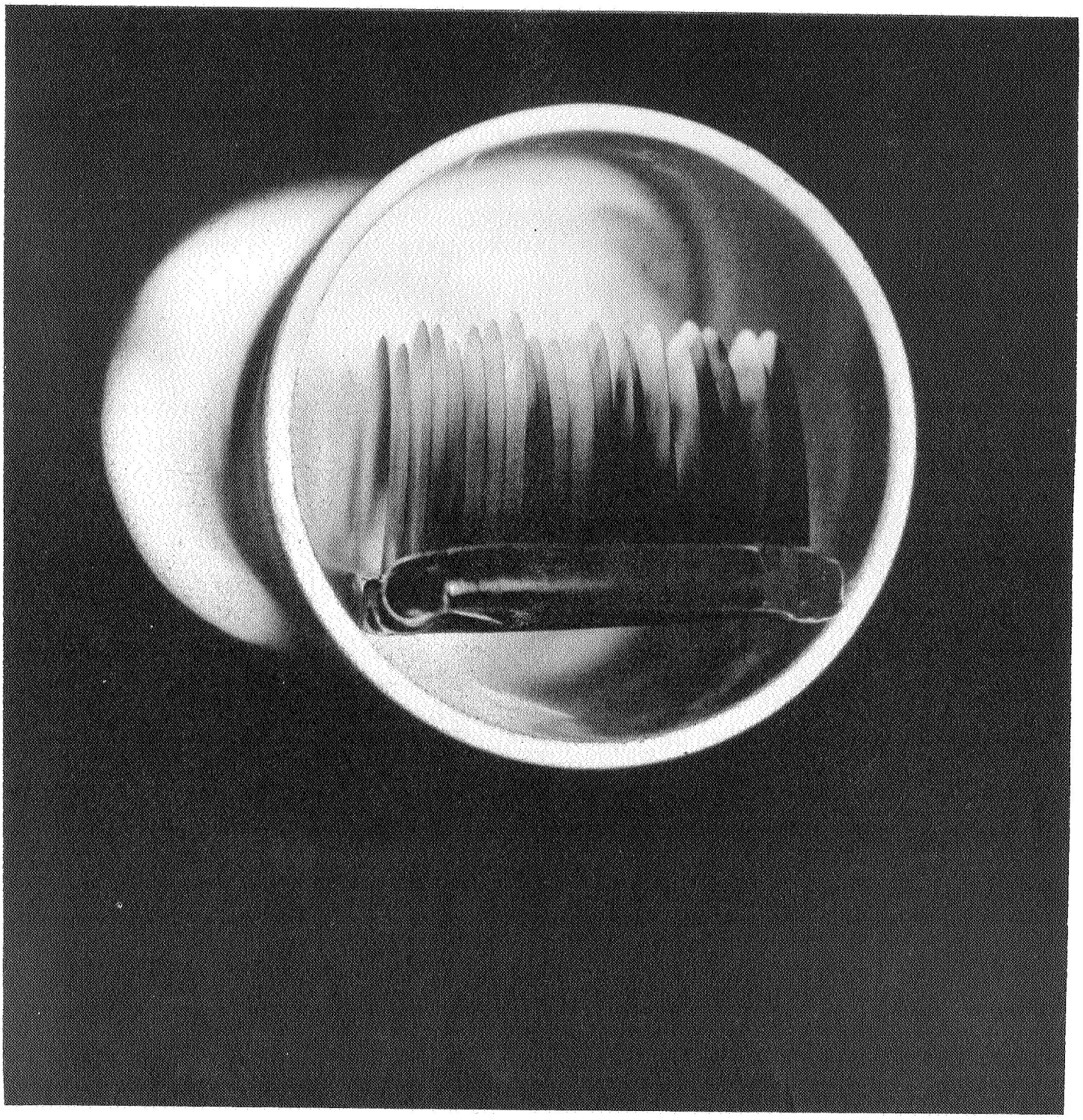


Fig. 3 Oxidation Furnace Loading

b. Dry Photoresist (1354) Rev. C dated 11-4-64

Coated wafers are air dired at 20° - 25°C for 25 - 30 minutes in a Laminar Flow Hood. They are then baked in nitrogen atmosphere at 90° C for 15 minutes. Equipment used is a Bake Oven and a Laminar Flow Hood; both manufactured by Fairchild.

c. Align and Expose Coated Wafers (1354) Rev. C dated 11-4-64

Wafers are aligned to the proper mask, brought into direct contact with the mask and exposed to high intensity ultraviolet light. Standard contact pressure is 10p/sq of nitrogen; light intensity for 4mw/cm^2 at 1050Å Typical exposure time is 5 seconds for 1μ KMER coatings. All operations are performed under a Laminar Flow Hood. Masks with scratches or missing patterns (as seen through the 35x alignment microscope), uncoated or broken wafers, or wafers too small to be held by the Alignment Jig are rejected. The Semi-automatic Alignment Jig, Laminar Flow Hood, and Ultraviolet Light Intensity Meter are manufactured by Fairchild. Exposure light intensity is set with the Ultraviolet Light Meter and calibrated by standards. Exposure time is set by the Develop Check Operator on the basis of a test wafer.

d. Develop Exposed Wafers (1925) Rev. O dated 1-11-65

Immerse exposed wafers in gently agitated Kodak Metal Etch Resist developer for 4 minutes, spray with electronic grade xylene for 30 seconds, immerse in trichloroethylene and Isopropyl alcohol solution (equal parts by volume) for 15 seconds, and blow wafers dry with clean dry nitrogen. Xylene, trichloroethylene, and isopropyl alcohol are manufactured by Mallinchrodt (Equivalents may be used.).

e. Develop Check (1925) Rev. O dated 1-11-65

THIS IS A CRITICAL INSPECTION STATION. Inspect wafers for alignment, exposure quality, line definition, develop completeness, photoresist adherence to the wafer, mask defects, pin holes in the photoresist, and scratches in the photoresist. Resistor widths are measured at 600x; all

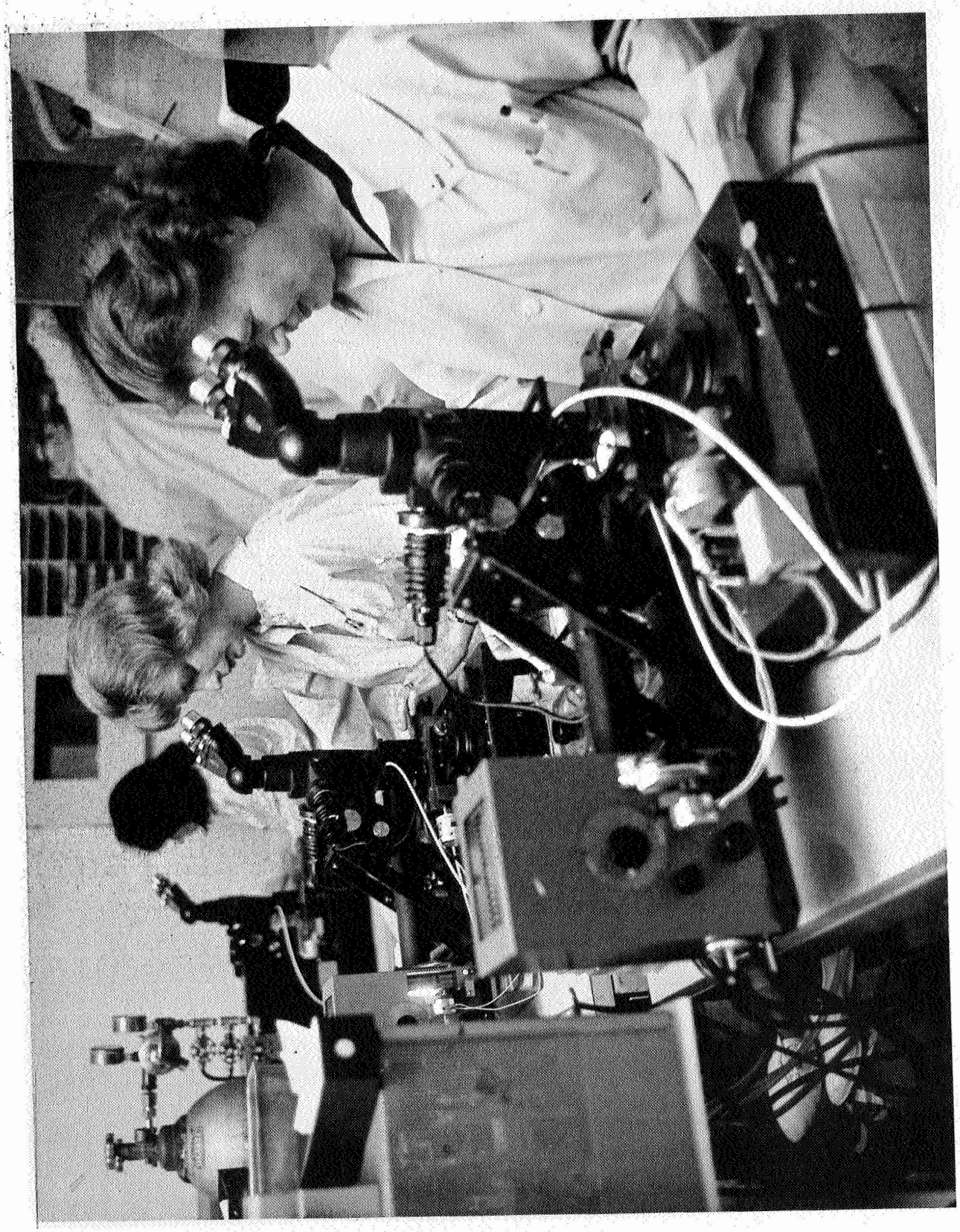


Fig. 4 Optical Alignment Jigs

inspections are made at 150x magnification or greater. THIS INSPECTION IS THE LAST POINT AT WHICH A WAFER MAY BE PROCESSED PRIOR TO ETCHING THE OXIDE. Misaligned patterns, incomplete or over exposure, i.e., enlarged or bridged lines, or photoresist lifting or peeling from the wafers is cause for rejection. Resistor tolerance of more than actual size +8% or less than actual size -12% is also cause for rejection. Photoresist may be stripped from the wafer at this point and reprocessed to correct any indicated problems. A Metallurgical Microscope (Bauch and Lomb), a Split Image Eyepiece (Watson, Inc.), and a Stage Micrometer (Bauch and Lomb) are used at this inspection station. The Split Image Eyepiece is calibrated with a Stage Micrometer for each lens to be used.

f. Oxide Etch (1926) Rev. O dated 3-18-65

The aligned and developed wafers are baked for 30 minutes at 150°C in a nitrogen atmosphere. The wafers are then immersed in oxide etch until all oxide is removed from the areas withou photoresist. Etch time is based on a test wafer from each lot. Wafers are rinsed in deionized running water for 15 minutes. Incomplete etching, i.e., broken lines or bridging, or over etching, i.e., severe undercutting of the photoresist is cause for rejection. Over etched wafers are discarded; under etched wafers are re-etched. Equipment used is a Laminar Flow Hood and Etch Tanks manufactured by Fairchild, and a Metallurgical Microscope manufactured by Bauch and Lomb.

g. Remove Photoresist (1360) Rev. A dated 12-29-64

To remove photoresist, wafers are immersed in chromic acid at 110°C ±10°C for 3 successive 5 minute baths. Wafers are then rinsed in isopropyl alcohol and blown dry with clean dry nitrogen. Wafers with remaining photoresist or water spots are rejected through the cleaning stage. The chromic cleaning station is Fairchild designed.

h. Final Check (1360) Rev. A dated 12-29-64

THIS IS A CRITICAL INSPECTION STATION. Wafers are inspected for cleanliness after photoresist removal. They are also inspected for the quality of the oxide etch, line

definition, completeness of etching, and over etching. AS THIS IS THE LAST INSPECTION PRIOR TO DIFFUSION, THE WAFER MUST BE CLEANED TO AVOID CONTAMINATION OF FURNACES AND OTHER WAFERS. Dirty wafers are recleaned. Incomplete or under etched wafers are remasked and re-etched; over etched wafers are discarded. A Laminar Flow Hood (Fairchild manufactured) and a Metallurgical Microscope (Bauch and Lomb) are used for this inspection station.

42. Predeposit and Diffuse Antimony (1924) Rev. O dated 11-11-64

THIS IS A CRITICAL INSPECTION STATION. Source material used is antimony trioxide. Furnace temperature is 1250°C; source temperature is 565°C. Wafers are furnaced for 2-1/2 hour cycles with a 2-1/2 minute 10:1 HF dip after each cycle. V/I is measured on a test chip and the average V/I is recorded. The V/I range is 3.0 - 5.0. V/I must be less than 5.0 to insure low R_{SAT} on circuit transistors. The lower V/I limit is used to check the process step control. If V/I does not lie in the range of 3.0 - 5.0, or, if visual inspection reveals contamination, the wafers are rejected and the materials, equipment and processing are closely examined to find the problem source. Equipment used in this process step is a Diffusion Furnace (Hevi-Duty Model HDH3736-5), a Source Furnace (Hevi-Duty Model M-1012-5), Fairchild manufactured V/I Measuring Equipment, and a Fairchild manufactured Laminar Flow Hood. Furnace temperature must be profiled at 1250°C ± 2°C. Source Furnace must be profiled at 565°C ±5°C.

43. First Re-Oxidation (1915) Rev. O dated 11-4-64

THIS IS A CRITICAL INSPECTION STATION. The furnace temperature is 1200°C ± 2°C. The steam generator is 3/4's full of deionized water at 90°C ± 1°C. The first re-oxidation cycle is 2 minutes in dry oxygen and 60 minutes in wet oxygen. The isolation diffusion cycle is one hour in dry oxygen and 30 minutes in wet oxygen. OXIDES MUST BE OF SPECIFIED THICKNESS FOR CONTROLLABLE OXIDE ETCHING, CORRECT SURFACE PROTECTION AND PASSIVATION. Oxides not of specified colors corresponding to desired oxide thickness are rejected. Equipment used is a Diffusion Furnace (Hevi-Duty Model HDH2726-5), a Voltage Adjustor (BKH No. 62564), a Heating Mantle (BKH No. 33787), a Laminar Flow Hood (Fairchild manufactured). Furnace temperature must be profiled at 1200°C ± 2°C.

44. Wafer Etch

Wafers are etched for three minutes in 100% HF acid to remove SiO_2. The wafers are then rinsed in DI H_2O for five minutes in each of three cascade rinse compartments, visually inspected, ultrasonically cleaned in DI H_2O for five minutes, dunked in isopropyl alcohol for two seconds, vapor degreased, blown dry with nitrogen and stored in desicators. The entire cleaning station is fabricated by Fairchild using a Branson Degreaser and an Ultrasonic Cleaning Tank and Generator (Acoustica Associates).

45. Grow Epitaxial Layer

A thin silicon layer is deposited on the wafers. The film is n-type 6 to 7 μ thick with a resistivity of .4Ω-cm. The layer is deposited by decomposing $SiCl_4$ at 1120°C ± 10°C in an Epitaxial Reactor and using phosphine as the n-type dopant. Wafers not meeting resistivity are rejected. Resistivity of the epitaxial layer is checked by a four-point probe measurement. The Epitaxial Reactor is manufactured by Fairchild and the four-point Probe is manufactured by A and M Fell, Ltd.

46. Measure Epitaxial Layer Thickness (1353) Rev. F dated 12-10-63

THIS IS A CRITICAL INSPECTION STATION. Thickness of the oxide layer is periodically checked by means of inter-parameter techniques. MAINTAINING PROPER OXIDE THICKNESS AND INTEGRITY IS NECESSARY TO OBTAIN THE PROPER FIRST STAGE ETCH. The etch can be altered if the thickness is known. A Zeiss Microscope is used for this measurement.

47. Second Re-Oxidation (1915) Rev. O dated 11-4-64

A protective layer of SiO_2 is grown on the epitaxial layer at 920°C ± 2°C for 2 hours in wet oxygen. Thin oxide coats are corrected by a temperature check of the furnace, steam generator furnace, and oxygen flow rate. The Diffusion Furnace used is a Model HDH3736-5 manufactured by Hevi-Duty. The furnace is profiled at 920°C ±2°C.

48. Final Process Inspection (2700) Rev. O dated 8-13-65

THIS IS A CRITICAL INSPECTION STATION. The wafers are inspected visually for oxide layer uniformity, pin holes, and variation of oxide thickness. PIN HOLES, FILM AND OXIDE THICKNESS VARIATIONS ON A SINGLE WAFER WILL CAUSE SERIOUS YIELD PROBLEMS AND INDICATE A PROCESS ERROR. Rainbow coloring of the wafers or light scattering spots indicate oxide layer thickness variations and is cause for rejection of the wafer. A Bauch and Lomb Microscope is used for this inspection.

49. Isolation Mask

All masking steps as in step no. 41.

50. Isolation Predeposition (1922) Rev. O dated 2-23-65

THIS IS A CRITICAL INSPECTION STATION. The source methyle borate is at -19°C ± 1°C. Furnace temperature is 1190°C. The cycle is 3 minutes followed by an 8 minute source flow. The wafers are soaked with source off. The V/I range of 0.5 - 1.2 is measured on a test chip and the results are recorded. V/I MUST BE LESS THAN 1.2 TO INSURE ISOLATION DIFFUSION THROUGH THE EPITAXIAL LAYER. The lower V/I limit is used to check process step control. Contaminated wafers and wafers outside the V/I limits are rejected. The equipment used is a Diffusion Furnace (Hevi-Duty Model HDH3736-5), V/I Measuring Equipment and a Laminar Flow Hood manufactured by Fairchild. Furnace temperature must be profiled at 1190°C ± 2°C.

51. Isolation Diffusion (1922) Rev. O dated 2-23-65

THIS IS A CRITICAL INSPECTION STATION. A p-type dopant is diffused through the n-type epitaxial layer until it reaches p-type substrate. This diffusion will isolate individual circuit components as required for the particular device. THE JUNCTION DEPTH MUST BE DEEPER THAN THE THICKNESS OF THE EPITAXIAL LAYER. Diffusion time is 1 hour in

dry oxygen followed by 1/2 hour in wet oxygen. The furnace used is manufactured by Hevi-Duty and the V/I measuring setup is fabricated by Fairchild. Furnace temperature is 1200° C ± 5° C and is profiled using a thermocouple and a potentiometer.

52. Base Mask (1354) Rev. C dated 11-4-64

All masking steps as in step no. 41.

53. Base Predeposition (1920) Rev. O dated 2-23-65

THIS IS A CRITICAL INSPECTION STATION. Boron atoms are deposited in the silicon wafer surface at 1020° C ±2° C. The source is boron trichloride. The cycle is 5 minutes heating followed by 30 seconds source time followed by 3 minutes 50 seconds source off time. V/I MUST BE IN THE RANGE OF 13 - 16 OHMS TO ENSURE CONTROL OF THE AMOUNT OF BORON DEPOSITED. THIS IS REFLECTED IN THE FINAL DEVICE CHARACTERISTICS AND RESISTOR VALUES. Equipment used is a Diffusion Furnace (Hevi-Duty HDH3736-5), a Laminar Flow Hood and a Four-Point Probe, both manufactured by Fairchild. Furnace temperature is profiled using a calibrated thermocouple and a potentiometer.

54. Base Diffusion (1921) Rev. O dated 2-12-65

THIS IS A CRITICAL INSPECTION STATION. Boron atoms are diffused into the silicon to form an electrical junction. A protective oxide is grown over the diffused layer. Temperature is 1175° C ±2° C. V/I MUST BE IN THE RANGE OF 24 - 28 OHMS TO ENSURE CONTROL OF THE FINAL DEVICE CHARACTERISTICS. OXIDE MUST BE OF A MINIMUM THICKNESS TO SUPPORT VOLTAGES USED. Wafers with V/I's outside the range of 24 - 28 ohms, or with oxides of less than a minimum of 4000Å thick are rejected. Equipment used is a Diffusion Furnace (Hevi-Duty HDH3736-5), a Four-Point Probe (V/I) and a Laminar Flow Hood, both manufactured by Fairchild. Furnace temperature is profiled using a calibrated thermocouple and potentiometer.

55. Emitter Mask (1354) Rev. O dated 2-23-65

All masking steps as in step no. 41.

56. Diode Check (1916) Rev. O dated 2-23-65

THIS IS A CRITICAL INSPECTION STATION. BV_{CBO} (collector-base voltage) is measured at 1 ma. THE COLLECTOR BASE DIODE IS AN ESSENTIAL STEP IN THE MANUFACTURE OF THE FINISHED DEVICE. Wafers with BV_{CBO} of less than 20 volts are rejected. Equipment used is a Model 6700 Curve Tracer, a 54x Optical Microscope, and a Three-Probe Jig, all Fairchild manufactured. The Curve Tracer is routinely checked by Fairchild;s Electronic Services Group.

57. Emitter Predeposition (1918) Rev. O dated 2-23-65

THIS IS A CRITICAL INSPECTION STATION. Phosphorus atoms are introduced and diffused into selected areas of the die at a temperature of 1080° C ± 2° C. THIS IS AN ESSENTIAL STEP IN DETERMINING THE FINAL DEVICE CHARACTERISTICS. Units with a V/I outside the range of 0. 55 = 0. 65 ohms are rejected. Equipment used is a Diffusion Furnace (Hevi-Duty HDH3736-5), a Four-Point Probe and a Laminar Flow Hood, both manufactured by Fairchild. Furnace temperature is profiled using a calibrated thermocouple and potentiometer.

58. Emitter Diffusion (1914) Rev. O dated 2-5-65

THIS IS A CRITICAL INSPECTION STATION. The emitter, after pre-deposition, is further diffused and an additional oxide is grown at a temperature of 1080° C ± 2° C. EMITTER DIFFUSION WILL DETERMINE THE FINAL DEVICE CHARACTERISTICS. V/I is checked to assure that it is in the range of 0. 52 - 0. 62. If outside the range of 0. 52 - 0. 62, the wafer is rejected. Equipment used is a Diffusion Furnace (Hevi-Duty HDH3736-5), a Laminar Flow Hood and a Four-Point Probe, both manufactured by Fairchild. Furnace temperature is profiled using a calibrated thermocouple and potentiometer.

59. Oxide Removal Mask (1354) Rev. C dated 11-4-64

All masking steps as in step no. 41.

60. Aluminum Evaporation (1927) Rev. A dated 4-29-65

THIS IS A CRITICAL INSPECTION STATION. Wafers receive a cleaning process including a 10:1 HF dip to remove residual SiO_2 remaining in the oxide windows. A tungsten filament is used for evaporation loaded to deposit aluminum of 99.9999% purity in a layer of $1\mu \pm 0.2\mu$ thickness. WAFERS MUST BE CLEAN DRY WHEN LOADED INTO THE EVAPORATION HOLDER. The evaporation is performed at a vacuum of at least 10^{-16} mm Hg as soon as possible after loading the wafers. V/I check of metal thickness ensures the reliability of metallization. Adherence is checked by applying a pressure sensitive tape to the evaporation film then removing the tape to check for peeling. THIS CHECK ENSURES THAT THE WAFERS HAVE BEEN PROPERLY CLEANED AND THAT THE METAL WILL ADHERE TO THE OXIDE. Wafers are rejected if (1) the metal is not of a proper thickness as measured by V/I tests; (2) adherence test reveals metal peeling; or (3) the metal is discolored although otherwise normal.

61. Metal Mask (1354) Rev. C dated 11-4-64

Masking Steps a through e (same as in step 41)

62. Metal Removal (1373) Rev. C dated 8-2-63

The wafers are placed in hot acid aluminetch (H_20-HNO_3-H_3PO_4) and etched until the patterns are clean and there is no bridging of leads. Etch temperature is $40°C \pm 5°C$. Wafers are then rinsed in deionized water in a three-stage cascade process of 5 minute/stage. Over or under etched leads are cause for rejection. Under etched leads are re-etched; over etched leads are stripped of all aluminum, recoated and re-masked. Equipment is a Hot Plateand a 3000 ml Pyrex beaker.

63. Remove Photoresist (Metal Mask) (1360) Rev. A dated 12-29-64

The wafers are immersed in J-100 photostrip, heated to 100° C ± 10° C, and agitated gently for 3 minutes. The wafers are then dipped in TCE for 1 minute, dipped in Acetone for 1 minute, dipped in isopropyl alcohol for 30 seconds, and cascaded rinsed. Wafers with remaining pho oresist or water spots are recleaned. Equipment used is a Hot Plate and a 3000 ml Pyrex beaker.

64. Quality Control Check (1925) Rev. O dated 1-11-65

THIS IS A CRITICAL INSPECTION STATION. Metal masking quality is checked and, if found defective, the metal is stripped and a new coat is evaporated. Oxide mask defects are checked and grossly defective wafers are rejected. Sporadic mask defects are counted and recorded as to the type of defects and number. A Bausch and Lomb microscope is used at this inspection station.

65. Aluminum Alloy (1917) Rev. O dated 2-24-65

THIS IS A CRITICAL INSPECTION STATION. The aluminum contacts are alloyed into the silicon and silicon oxide layers to provide a ohmic contact and to bond the aluminum to the die at a temperature of 560° C ± 2° C. ALUMINUM MUST ADHERE TO THE DIE AND PROVIDE OHMIC CONTACT TO THE DIE IN ORDER TO GIVE GOOD R_{SAT} CHARACTERISTICS. Wafers are rejected if R_{SAT} is outside the specified range for the intended device. Equipment used is an Alloy Furnace (Hevi-Duty HDH3736-5), a Model 6200 Curve Tracer, a 45x Optical Microscope and a Two-Probe Jig, all manufactured by Fairchild. Furnace temperature is profiled using a calibrated thermocouple and potentiometer. The Curve Tracer is routinely calibrated by Fairchild's Electronic Services Group.

66. Electrical Check (T-84)

THIS IS A CRITICAL INSPECTION STATION. Electrical parameters are tested on finished wafers; i. e., beta, LV_{CED}, BV_{CES}, resistors. THIS TEST QUICKLY ILLUSTRATES WHETHER

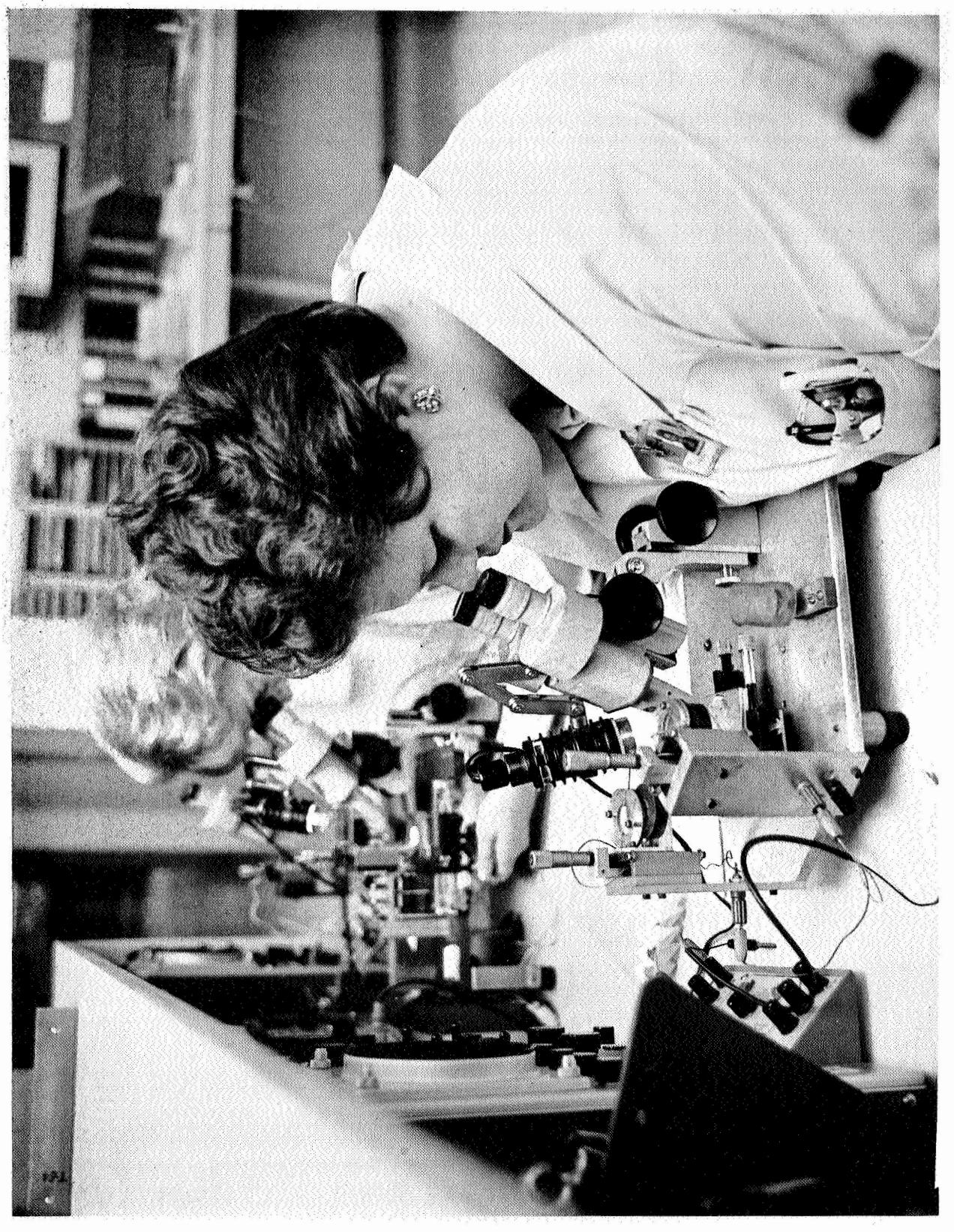


Fig. 5 Electrical Test (T-84) Jig

THE ABOVE CIRCUIT PARAMETERS ARE WITHIN THE SPECIFIED LIMITS FOR THE INTENDED DEVICE. Wafers outside of specified limits are rejected. Equipment used is a Curve Tracer and a Probe Set, both manufactured by Fairchild.

67. Electrical Wafer Sort (1546) Rev. C dated 1-22-64

All dice are DC tested on the wafer. Dice that do not pass specified parameter limits are rejected. Equipment used is a Automatic Wafer Sorter and a 4000M Tester, both manufactured by Fairchild.

68. Scribe and Break (1795) Rev. O dated 7-7-64

Lines are scribed between dice on the wafer to separate into individual dice. The scribe and break station is fabricated by Fairchild (Dwg. No. 12345D).

69. Visual Die Sort (Second Optical Inspection) (1982) Rev. A dated 6-8-65

THIS IS A CRITICAL INSPECTION STATION. All electronically good dice are 100% inspected for optical defects detrimental to device performance and reliability. The Inspection Jig used at this station is fabricated by Fairchild.

70. Purchase Bases

Quality Control inspected glazed bases are purchased from the materials department.

71. Purchase Frames

Quality Control inspected aluminum evaporated frames are purchased from the materials department.

72. Purchase Caps

Quality Control inspected glazed caps are purchased from the materials department.

73. Automatic Die Attach (1891) Rev. O dated 2-1-65

Visually inspected dice are attached to a CERPAK Base. The bases are heated on heater blocks until the glass melts. The frame is then placed in position on the base and the die is scrubbed until it is held firmly in the cavity of the base. Cracked or chipped dice, glass covered dice, and dice which are mislocated or misoriented in the cavity are rejected and the vacuum pick-up is readjusted according to the position of the microscope for shipped dice. Vacuum control must be closely monitored. Equipment used is a Die Attach Jig with Microscope and Timer, a Frame Rack, Stainless Steel Tweezers, a Brush and a Screw Driver, all manufactured by Fairchild. The temperature of the heater block is measured by a thermocouple and varies according to glass thickness.

74. Ultrasonic Bonding (1892) Rev. O dated 2-1-65

Aluminum wire connections are made between the die bonding pads and the aluminized leads. Bridging bonds, unattached bonds, tails, flat bonds, misconnections, damaged wire, looped wire, and/or Kovar contact is cause for rejection. Equipment used is an Ultrasonic Bonder (Fairchild Dwg. No. 18104E), Aluminum Wire (to Spec 9178-2), an Ultrasonic Bonding Tool (Tempress Research Dwg. No. 17320 C), and Stainless Steel Tweezers.

75. Wash CERPAK Sub-Assemblies (1893) Rev. O dated 2-1-65

CERPAK sub-assemblies are cleaned before sealing. If aluminum "wash-out" in the base cavity occurs, the die is inspected for bridging at 45x magnification and the deionized water is sample tested for contamination. Sample testing of the deionized water is a routinely performed inspection check. The complete Wash Station is fabricated by Fairchild.

76. Pre-Seal Inspection (Third Optical Inspection) (1567) Rev. C dated 11-14-63

THIS IS A CRITICAL INSPECTION STATION. The sub-assembly

units are visually inspected at 45x magnification for bond location on the die, die, base, and frame. All sub-assembly units are screened for reliability defects prior to final seal. A Microscope (American Optical Co. or Bausch and Lomb) is used at this inspection station.

77. Quality Control Check (1899) Rev. B dated 4-9-65

All dice are checked for ultrasonic bonding defects and for adherence tothe third optical inspection. The test jig used at this station is fabricated by Fairchild.

78. Final Seal

Sub-assembled units are hermetically sealed and visually inspected for sealing defects. The equipment used is a Devitrification Furnace (RCK) and quartz boats. The furnace is profiled weekly using a potentiometer and a thermocouple.

79. Gold Plating

Device leads are gold plated for rust protection, conductivity, and solderability.

80. Optical Inspection (Gold Plating)

Device leads are visually inspected to assure uniform plating quality. Devices with non-uniform plating quality are re-plated.

81. Optical Inspection after Final Seal (1567) Rev. C dated 11-14-65

THIS IS A CRITICAL INSPECTION STATION. After final sealing of the CERPAK package, optically poor units are rejected. Glass seals, alignment, ceramics and frame qualities are inspected to ensure that only good hermetically sealed units continue to gold plating process steps. Units with holes in seal, cold seal, excessive glass, defective ceramic, misalignment, and

mangled frames are rejected. Equipment used is a Low Power Microscope (American Optical Co.) and Gauge Blocks manufactured by Fairchild.

82. Temperature Cycle (1734) Rev. O dated 5-14-64

Thermal shock is applied to destroy marginal defects. Thermally stressed packages will be rejected at Radiflo. Equipment used is an Oven (Missimers Inc. Model 3-62-200C), a Temperature Shock Chest (Missimers Inc.), and a Timer (BKH No. 62371), and a Fan (General Electric).

83. Centrifuge Test (1718) Rev. O dated 10-12-63

The packages are capability tested to withstand centrifuge tests at approximately 20,000g in x1 or x2 directions. Mechanical stresses and strains will result in fissures in the seal which will be detected at Radiflo; weak bonds will be broken. The centrifuge used is a Model K (Dwg. No. SKC-2779) and a 2936 Double Deck Rotor, both manufactured by Beckman Spin Co.

84. Radiflo (5039) Rev. A dated 3-20-63

THIS IS A CRITICAL INSPECTION STATION. Sealed units are subjected to krypton gas at calculated pressure, time and temperature to ensure hermetic seal of the package. Units with leaks through the seal or package are rejected. Radiflo equipment is manufactured by the American Nuclear Co.

85. Gross Leak Bubble Test (1733) Rev. A dated 7-17-64

Units are tested to detect gross leaks in the packages through bubble emmission from cavity through holes. Units with leaks are rejected. Equipment and materials used are mineral oil with a viscosity range of 175 - 190 seconds at 38°C, a quart Pyrex pan, a hot plate, a 159°C thermometer, and a Magnetic Device Holder manufactured by Luxo-Lite.

86. Final Device Classification

THIS IS A CRITICAL INSPECTION STATION. Packaged devices are DC tested to assure that they pass specified limits. Equipment used at this test station is a Multi-Probe Tester and a 4000M Tester, both manufactured by Fairchild.

87. Quality Assurance Inspection

Quality Assurance checks finished devices per Special Logic (SL) Specifications to customer limits and requirements. A Fairchild 4000 Tester is used at this station along with an oscilloscope to check switching times.